DETAILED ACTION

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1 and 3-4 rejected under 35 U.S.C. 101 because the claimed invention is

directed to non-statutory subject matter. Claims 1 and 3-4 recite a method for

accelerating input bit flow without reciting any hardware or performing a transformation

on a tangible and physical article; furthermore, the claims recite factors weighing

against eligibility as described in the Interim Guidance for Determining Subject Matter

Eligibility for Process Claims in View of Bilski v. Kappos dated July 27, 2010. The

factors including: The claim is a general concept of delaying an input and combining the

delayed input to generate an output, the claims recite a general concept that is

disembodied, and lastly the mechanisms by which the steps are implemented are

subjective. Therefor claims 1 and 3-4 are directed to non-statutory subject matter under

35 USC 101.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 5-9 rejected under 35 U.S.C. 102(b) as being anticipated by Ailett

et al. (US 3,881,099) (hereinafter Ailett).

As per claim 1, Ailett discloses a method for accelerating a pseudo-random input

bit flow (PRBS(T.sub.1)), generated at a first relatively low dock frequency (f1) (Column

1, lines 46-52, the input is at the frequency of the generator), into an identical output bit

flow (PRBS(T.sub.0)) at a second relatively high clock frequency (Column 1, lines 61-

63) (f0), comprising: collecting the output bit flow; delaying the collected flow by a

predetermined value (.tau.); and combining the delayed flow with the input bit flow

(Column 1, 53-68, the input is collected, delayed by half the input frequency, combined

by a multiplexer, and output at twice the input frequency), wherein delay T is selected to

respect the following relation: .tau.=2.sup.IT.sub.1-T.sub.0,where T.sub.1 represents the

dock period of the input bit flow, T.sub.0 represents the dock period of the output bit

flow, and I is an integer setting a decimation parameter (Column 1, lines 53-67, when

tau is $.5T_1$ or (N/2), the delay is half the input frequency (sample length) for L=0, $2T_0 = T_1$

and tau=$.5T_1$).

As per claim 5, it is the circuit implementing the method of claim 1, therefor it is

rejected under the same rationale.

As per claim 6, Ailett discloses the circuit of claim 5, wherein a reshaping

element at the high frequency is provided at the combiner output (Column 2, lines 36-

64, the time multiplexer receives the input and a phase shifted input for combination at

the higher frequency).

As per claim 7, Ailett discloses the circuit of claim 5, wherein a phase-shifting

element is further provided between the generator of the original pseudo-random bit

sequence and the combiner (Column 2, lines 36-64, the time multiplexer receives the

input and a phase shifted input for combination at the higher frequency).

As per claim 8, Ailett discloses the circuit of claims 5, wherein the initial bit flow is

obtained by a flip flop generator (Column 1, lines 22-30, flip-flops generate the

pseudorandom sequence).

As per claim 9, Ailett discloses the circuit of claim 5, formed by optical and/or

electronic means (Column 1, lines 22-30, flip-flops generate the pseudorandom

sequence where flipflops and multiplexors are electrical circuits).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-4 rejected under 35 U.S.C. 103(a) as being unpatentable over Ailett.

As per claim 3, Ailett discloses the method of claim 1, wherein delay .tau. is selected to respect the following relation: .tau.=(2k+1)*(2.sup.n-1)*T.sub.0,where k represents any integer, and where n represents the degree of the irreducible polynomial of the random sequence (Column 2, lines 38-50, when k=0 the equation delay=(number of samples)*(output frequency) is generated as qF when every flipflop is output is connected).

Ailett fails to expressly disclose tau.=(2k+1)*(2.sup.n-1)*T.sub.0,where k represents any integer, where the integer is a number other than zero.

However, Calculations of the rate show that term (2K+1) cancels out when determining the delay required for input and output ratios to be established. Effectively showing (2K+1) could be replaced with any term and yield the same results. Since the applicant has failed to disclose that (2K+1) is used for a particular purpose, or solves a stated problem, it would have been an obvious matter of *design choice* to insert (2K+1) into the equations.

As per claim 4, Ailett discloses the method of claim 3, wherein numbers k and l respect the following relation: (2k+1)*(2.sup.n-1)+1=p2.sup.l,where p is the desired acceleration factor (Column 1 lines 53-67 and Column 2 lines 38-50, when k=0, the desired acceleration factor is T_1/T_0 or the factor that the output frequency is scaled to [f=1/t]).

Ailett fails to disclose $(2k+1)*(2^{n}-1)+1=p2^{l}$ where k represents any integer, where the integer is a number other than zero.

However, Calculations of the rate show that term (2K+1) cancels out when determining the delay required for input and output ratios to be established. Effectively showing (2K+1) could be replaced with any term and yield the same results. Since the applicant has failed to disclose that (2K+1) is used for a particular purpose, or solves a stated problem, it would have been an obvious matter of *design choice* to insert (2K+1) into the equations.

Response to Arguments

Applicant's arguments filed 3/28/2011 have been fully considered but they are not persuasive.

Applicant argues on pages 7-8 for claims 1 and 3-4 that they should not be rejected under 35 USC 101 because of factors from Federal Circuit 2010-1037.

The examiner respectfully submits that the case law is not applicable to the instant claims because the case law recites on page 15:

> "The fact that some claims in the '310 and '228 patents require a "high contrast film," "a film printer," "a memory," and "printer and display devices" also confirm this court's holding that the invention is not abstract. Indeed, this court notes that inventions with specific applications or improvements to technologies in the marketplace are not likely to be so abstract that they override the statutory language and framework of the Patent Act. "

The present invention can be implemented without any specific hardware such as determined to override the statutory requirements of the cited case law. Software is capable of capturing an input stream delaying it and outputting a new stream. Even further two individuals could perform the same sequence of steps. Lastly, the claims recite factors weighing against eligibility as described in the Interim Guidance for Determining Subject Matter Eligibility for Process Claims in View of Bilski v. Kappos dated July 27, 2010. The factors including: The claim is a general concept of delaying an input and combining the delayed input to generate an output, the claims recite a general concept that is disembodied, and the mechanisms by which the steps are implemented are subjective. The claims do not detail a particular apparatus for performing the steps, only a general purpose device.

Applicant argues on pages 9-12 that the prior art fails to recite that L is an integer, therefor the claims are allowable over the prior art.

The examiner respectfully submits that the rejection contained a typo "when 1 is .5 or n/2" The examiner uses the numeric 'one' which should have been greek 'tau'. The applicant perceived the numeric 'one' as lower case 'L'. In order for $2T0=T1$ to hold true as stated in the office action, L must be zero. (While not cited previously, the prior art also holds for L=3) Therefor, L is an integer as applied in the prior art.

Applicant argues on pages 9-12 that the prior art fails to recite tau = 2^l T1-

T0, therefor the claims are allowable over the prior art.

The examiner respectfully submits that while the examiner may cite

sections of the prior art for teaching limitations that the entire prior art as a

whole must be considered. In column 2, lines 38-64 further disclose that

the delay is set off of qF or 2^h multiplied by the input frequency mod the

output frequency where the output frequency is qF and the input

frequency is F. Further the delay flip flops in q sum are modulous 2 circuits

(for setting the delay 2^k). Therefor, the delay sets the output at a multiple

of the input frequency, or a decimation factor for choosing the ration of the

delayed output to input.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to KEVIN HUGHES whose telephone number is (571)270-

3365. The examiner can normally be reached on M-Th/F 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Lewis Bullock can be reached on 5712723759. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lewis A. Bullock, Jr./   /KEVIN HUGHES/
Supervisory Patent Examiner, Art Unit 2193   Examiner, Art Unit 2193